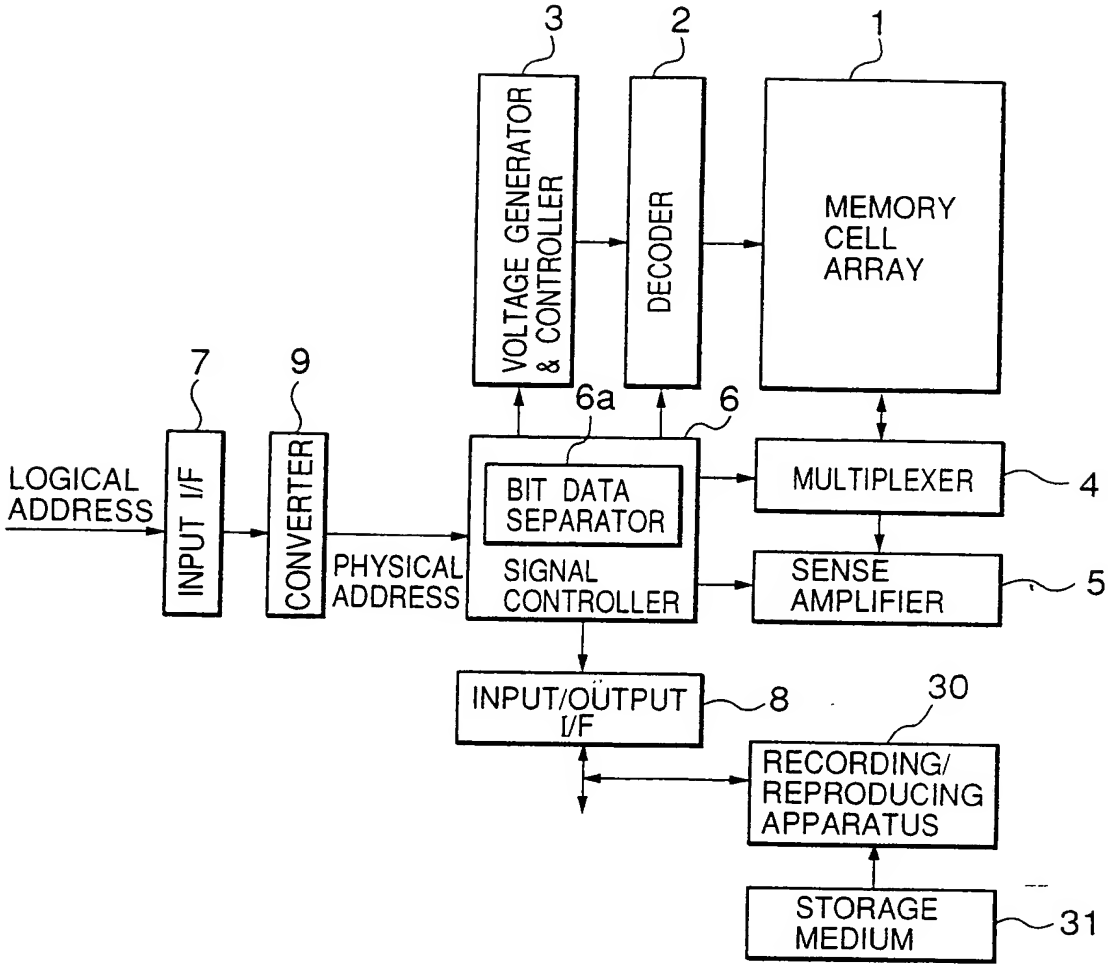
3
2
1
VOLTAGE GENERATOR & CONTROLLER
DECODER
MEMORY CELL ARRAY
7
9
6a
6
LOGICAL ADDRESS
INPUT I/F
CONVERTER
PHYSICAL ADDRESS
BIT DATA SEPARATOR
SIGNAL CONTROLLER
MULTIPLEXER
4
SENSE AMPLIFIER
5
INPUT/OUTPUT I/F
8
30
RECORDING/ REPRODUCING APPARATUS
STORAGE MEDIUM
31

FIG.1

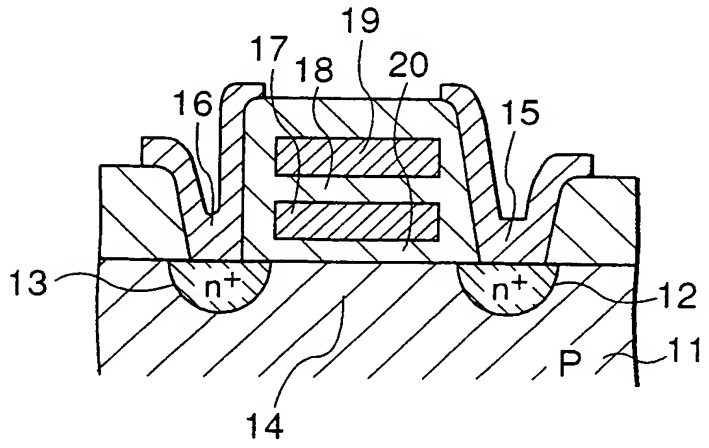
19
17
18
20
16
15
13
n+
n+
12
P
11
14

FIG.2

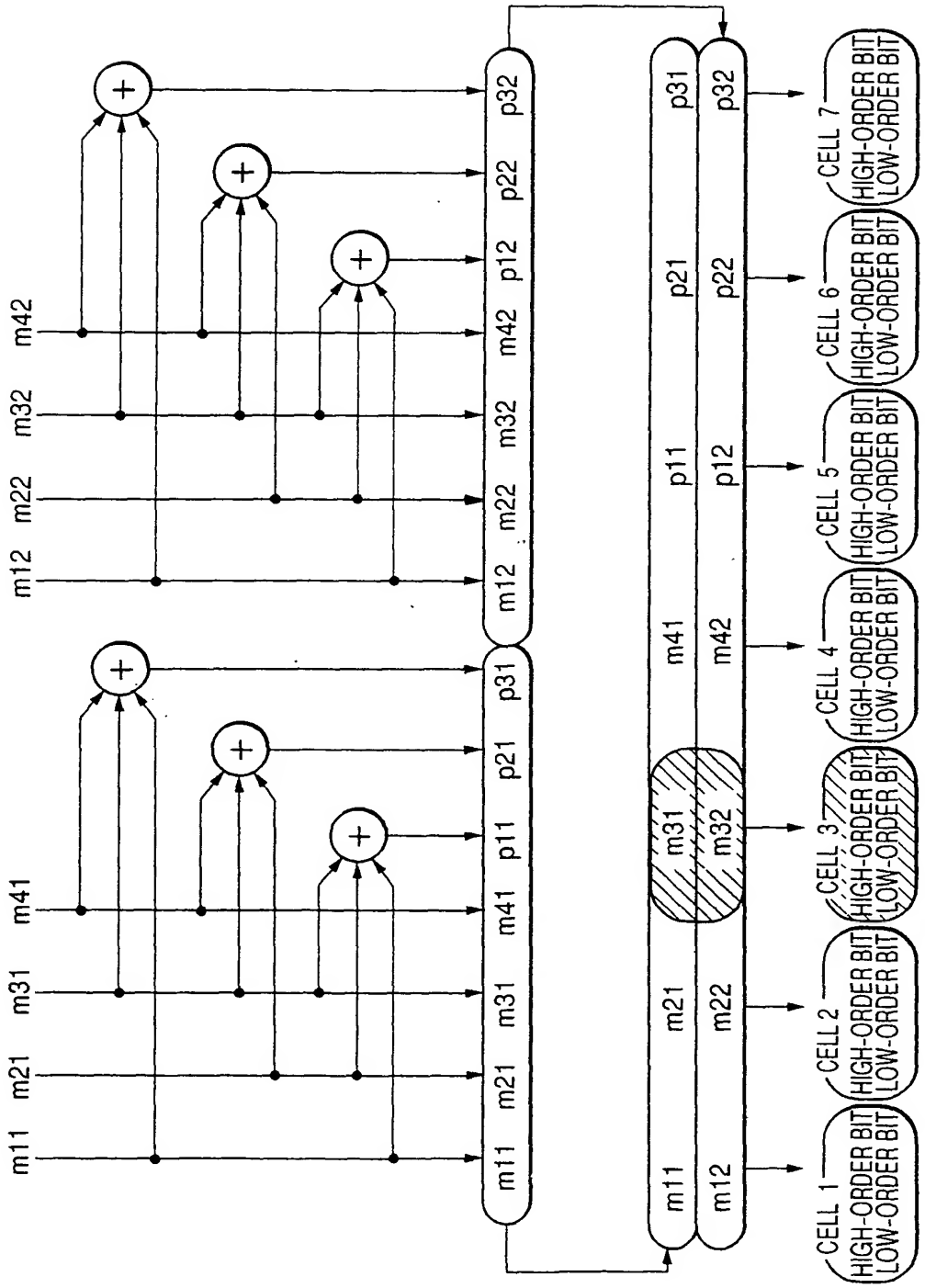
m11
m21
m31
m41
m12
m22
m32
m42
m11 m21 m31 m41 p11 p21 p31 p12 m12 m22 m32 m42 p12 p22 p32
m11 m21 m31 m41 p11 p21 p31 p12 m12 m22 m32 m42 p22 p32 p31
m11 m12 m21 m22 m31 m32 m41 m42 p11 p12 p21 p22 p31 p32
CELL 1
CELL 2
CELL 3
CELL 4
CELL 5
CELL 6
CELL 7
HIGH-ORDER BIT
LOW-ORDER BIT

FIG.3

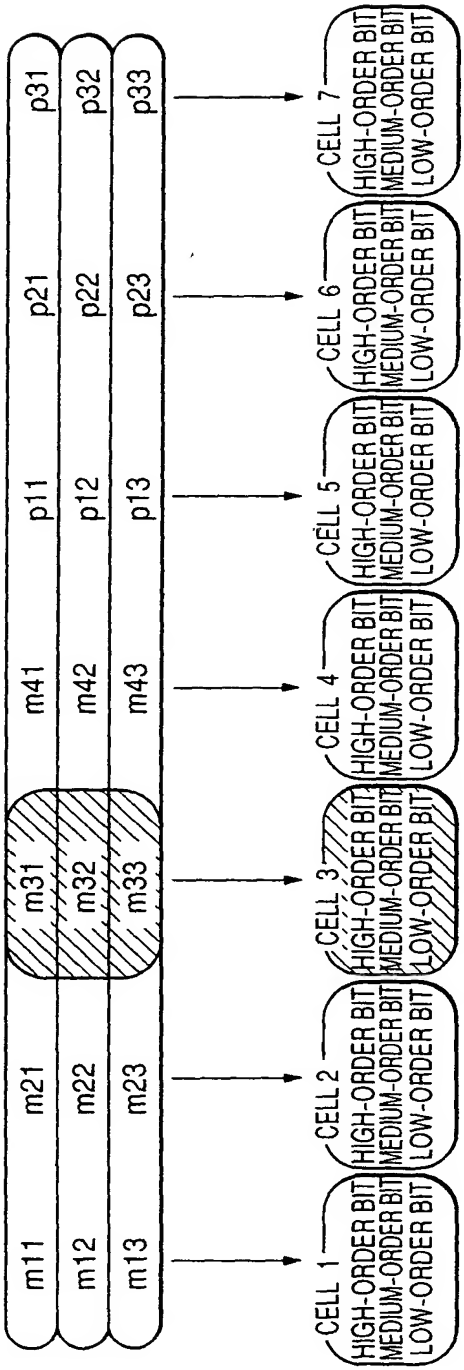
m11
m21
m31
m41
p11
p21
p31
m12
m22
m32
m42
p12
p22
p32
m13
m23
m33
m43
p13
p23
p33
CELL 1
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 2
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 3
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 4
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 5
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 6
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 7
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT

FIG.4

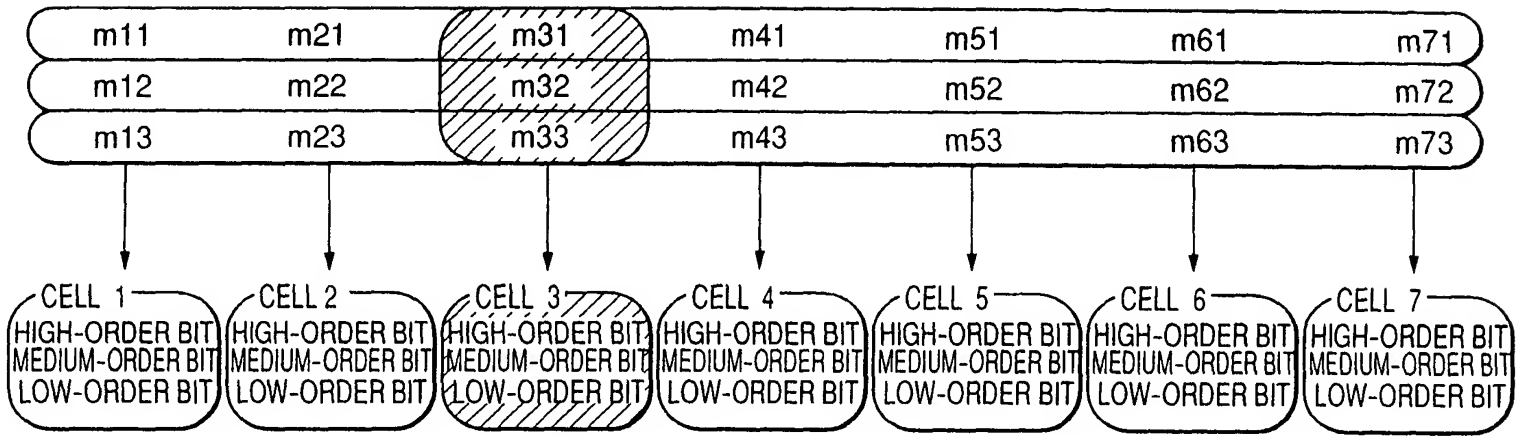
m11 m21 m31 m41 m51 m61 m71
m12 m22 m32 m42 m52 m62 m72
m13 m23 m33 m43 m53 m63 m73
CELL 1
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 2
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 3
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 4
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 5
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 6
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 7
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT

FIG.5A

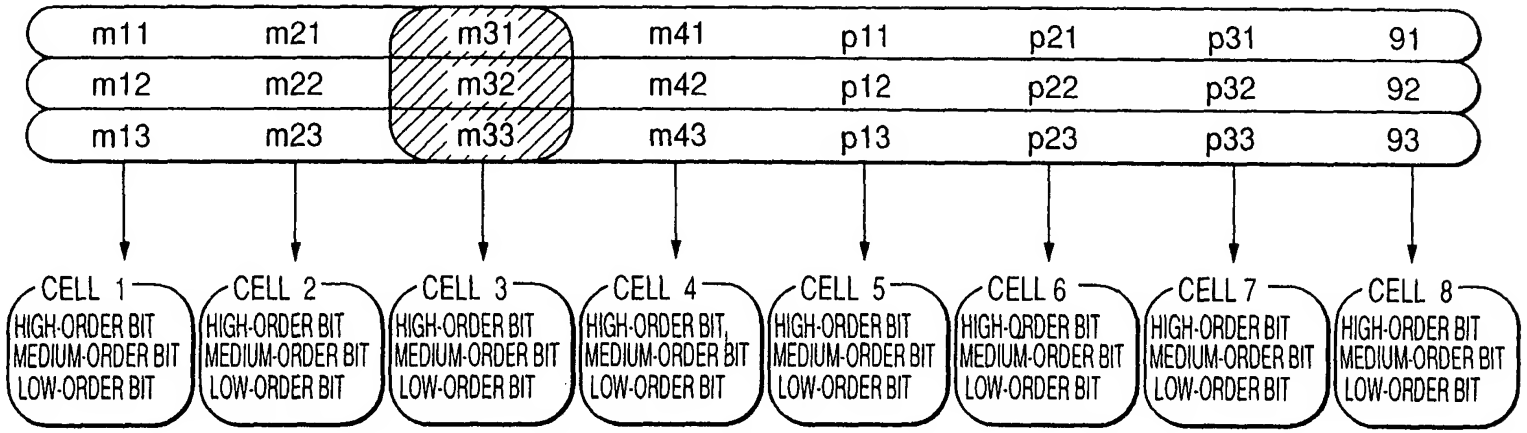
m11 m21 m31 m41 p11 p21 p31 91
m12 m22 m32 m42 p12 p22 p32 92
m13 m23 m33 m43 p13 p23 p33 93
CELL 1
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 2
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 3
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 4
HIGH-ORDER BIT,
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 5
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 6
HIGH-QRDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 7
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT
CELL 8
HIGH-ORDER BIT
MEDIUM-ORDER BIT
LOW-ORDER BIT

FIG.5B

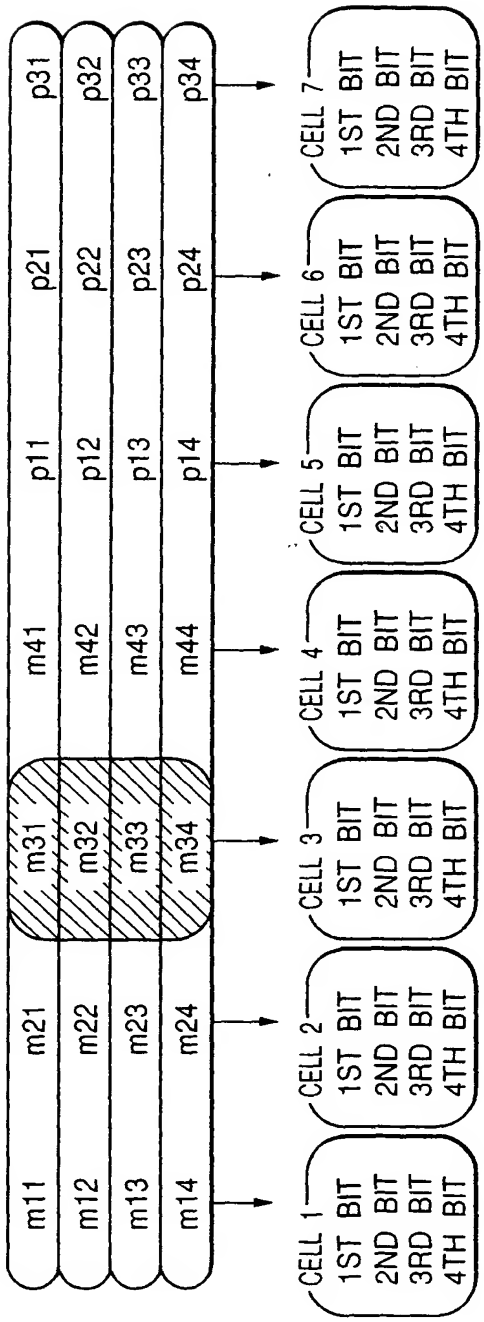
m11
m12
m13
m14
m21
m22
m23
m24
m31
m32
m33
m34
m41
m42
m43
m44
p11
p12
p13
p14
p21
p22
p23
p24
p31
p32
p33
p34
CELL 1
1ST BIT
2ND BIT
3RD BIT
4TH BIT
CELL 2
1ST BIT
2ND BIT
3RD BIT
4TH BIT
CELL 3
1ST BIT
2ND BIT
3RD BIT
4TH BIT
CELL 4
1ST BIT
2ND BIT
3RD BIT
4TH BIT
CELL 5
1ST BIT
2ND BIT
3RD BIT
4TH BIT
CELL 6
1ST BIT
2ND BIT
3RD BIT
4TH BIT
CELL 7
1ST BIT
2ND BIT
3RD BIT
4TH BIT

FIG.6

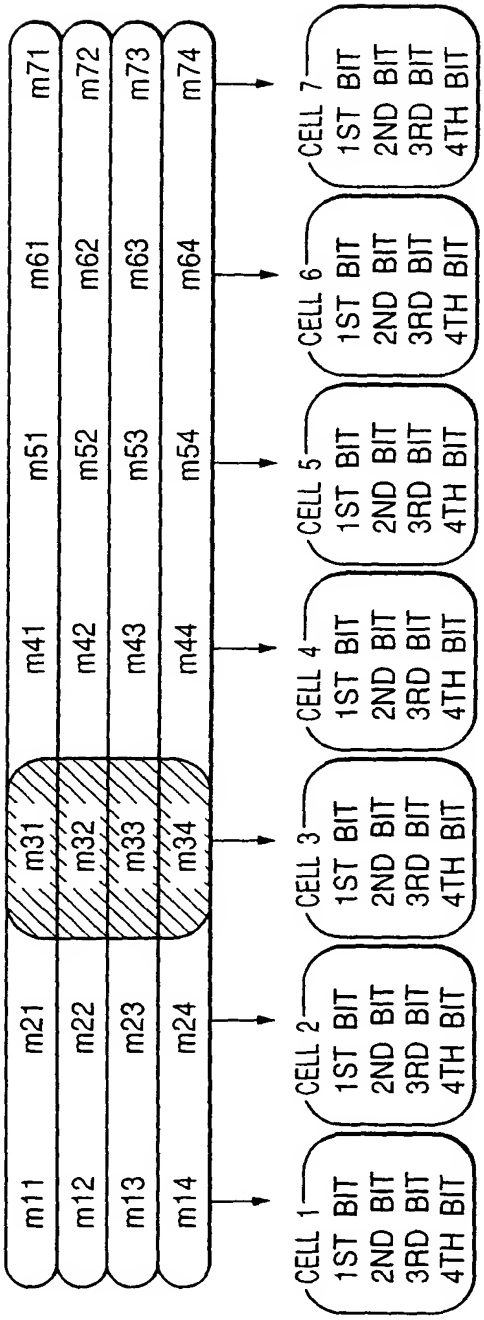
m11 m21 m31 m41 m51 m61 m71
m12 m22 m32 m42 m52 m62 m72
m13 m23 m33 m43 m53 m63 m73
m14 m24 m34 m44 m54 m64 m74
CELL 1 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 2 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 3 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 4 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 5 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 6 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 7 1ST BIT 2ND BIT 3RD BIT 4TH BIT

FIG.7A

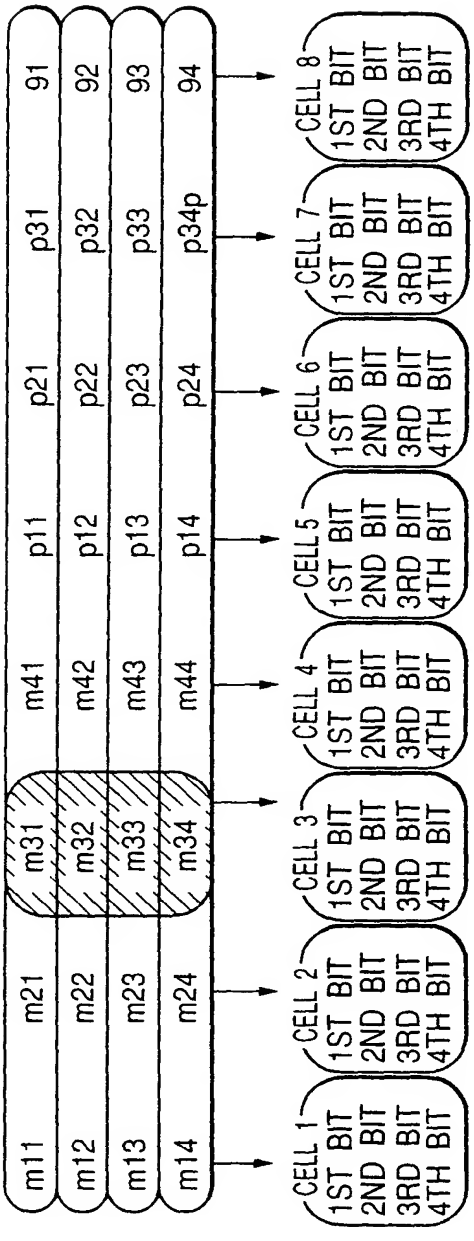
m11 m21 m31 m41 p11 p21 p31 91
m12 m22 m32 m42 p12 p22 p32 92
m13 m23 m33 m43 p13 p23 p33 93
m14 m24 m34 m44 p14 p24 p34p 94
CELL 1 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 2 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 3 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 4 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 5 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 6 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 7 1ST BIT 2ND BIT 3RD BIT 4TH BIT
CELL 8 1ST BIT 2ND BIT 3RD BIT 4TH BIT

FIG.7B

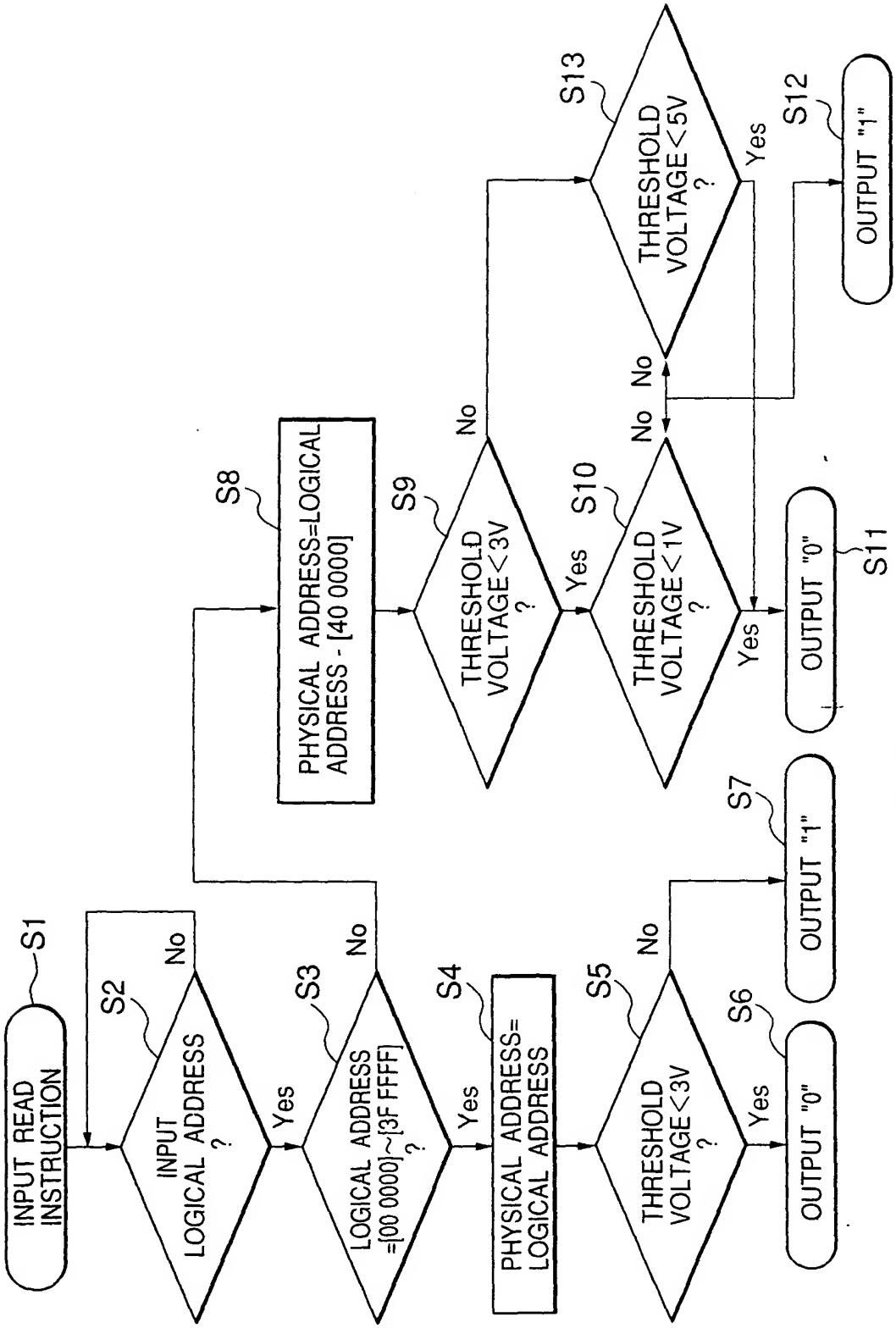
INPUT READ INSTRUCTION
S1
INPUT LOGICAL ADDRESS ?
S2
No
Yes
LOGICAL ADDRESS =[00 0000]~[3F FFFF] ?
S3
No
Yes
PHYSICAL ADDRESS= LOGICAL ADDRESS
S4
THRESHOLD VOLTAGE<3V ?
S5
No
Yes
OUTPUT "0"
S6
OUTPUT "1"
S7
PHYSICAL ADDRESS=LOGICAL ADDRESS - [40 0000]
S8
THRESHOLD VOLTAGE<3V ?
S9
No
Yes
THRESHOLD VOLTAGE<1V ?
S10
No
Yes
OUTPUT "0"
S11
THRESHOLD VOLTAGE<5V ?
S13
No
Yes
OUTPUT "1"
S12

FIG.8

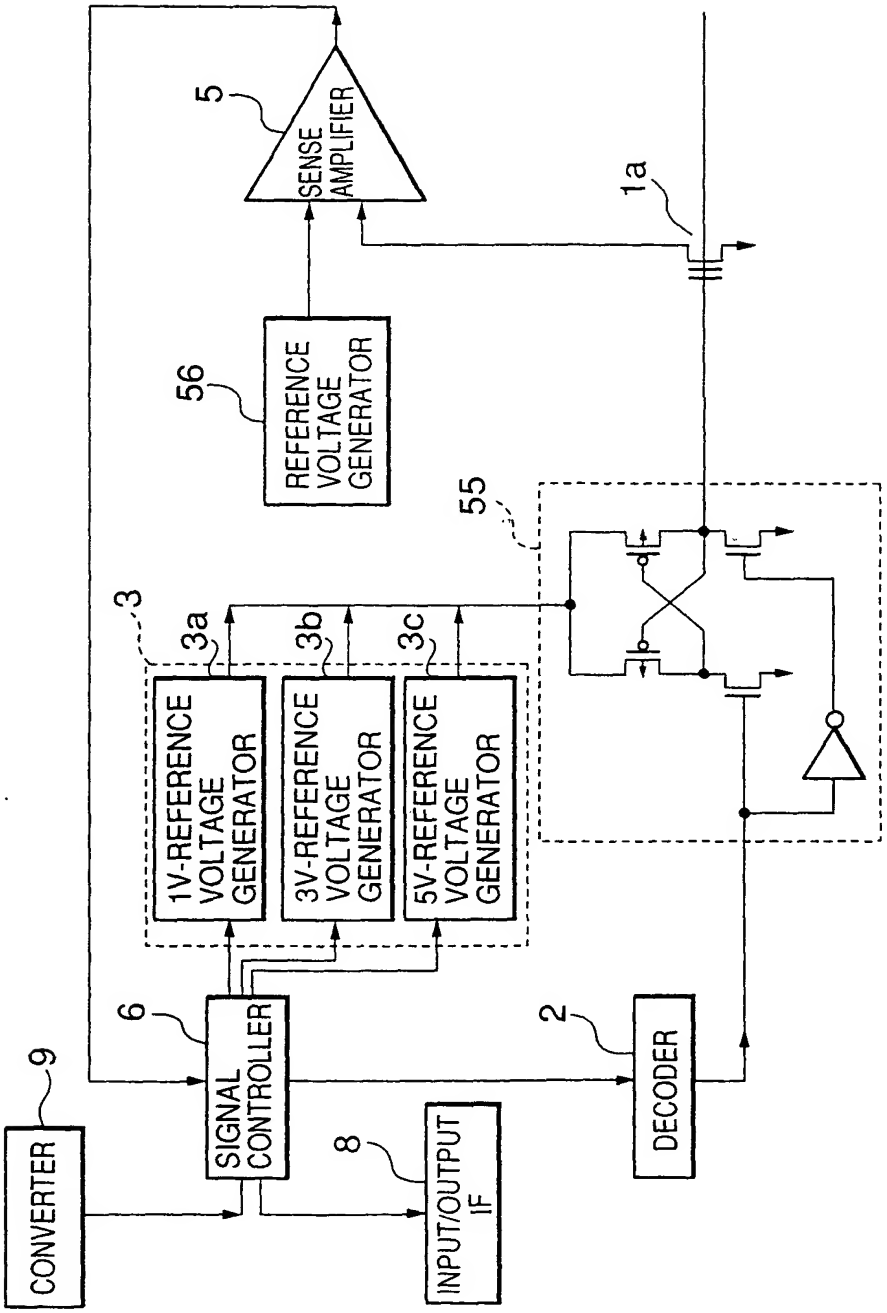
CONVERTER
9
SIGNAL CONTROLLER
6
INPUT/OUTPUT IF
8
DECODER
2
1V-REFERENCE VOLTAGE GENERATOR
3V-REFERENCE VOLTAGE GENERATOR
5V-REFERENCE VOLTAGE GENERATOR
3
3a
3b
3c
55
REFERENCE VOLTAGE GENERATOR
56
SENSE AMPLIFIER
5
1a

FIG.9

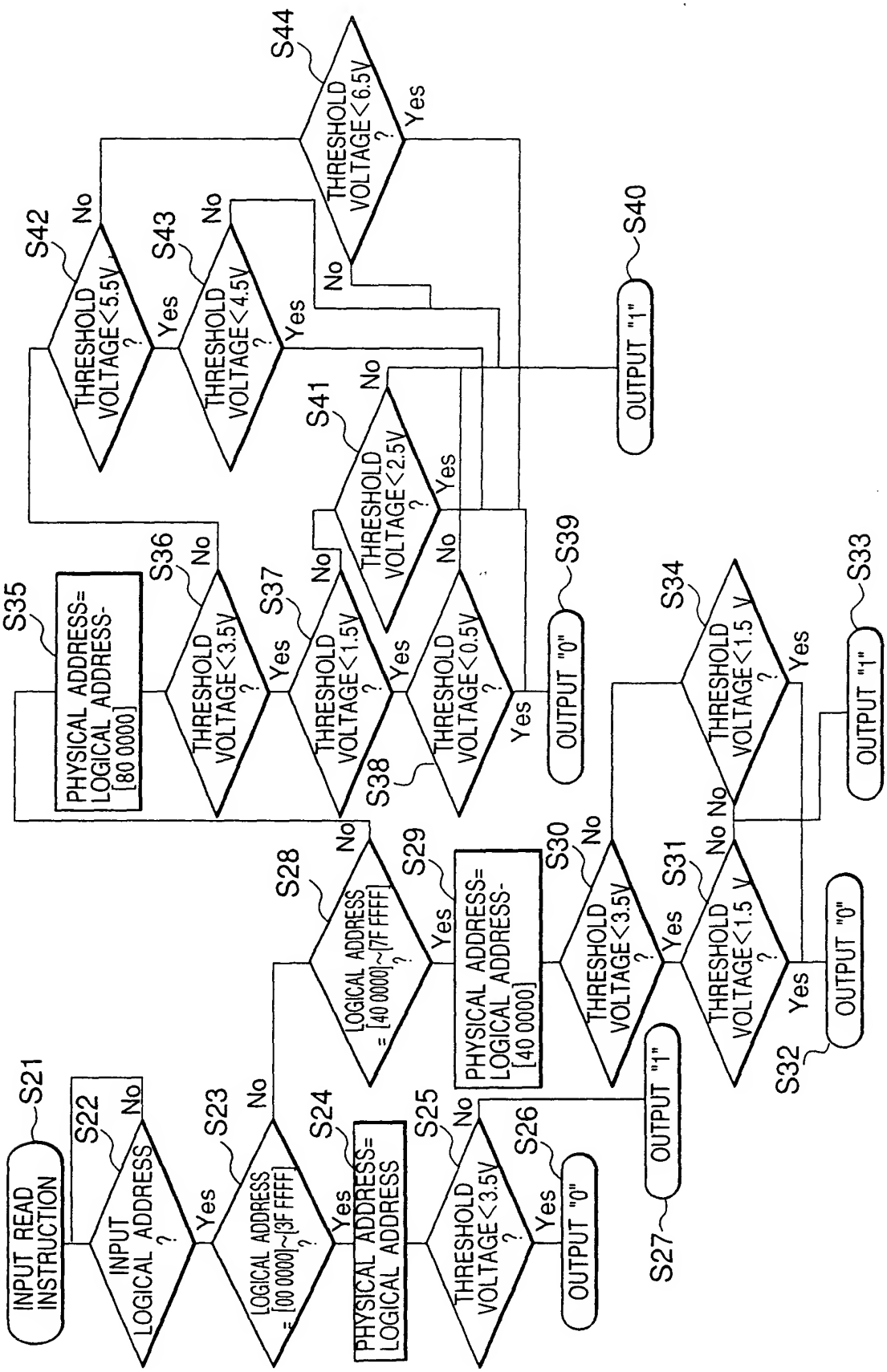
INPUT READ INSTRUCTION
S21
INPUT LOGICAL ADDRESS ?
S22
No
Yes
LOGICAL ADDRESS = [00 0000]~[3F FFFF] ?
S23
No
Yes
PHYSICAL ADDRESS= LOGICAL ADDRESS
S24
THRESHOLD VOLTAGE<3.5V ?
S25
No
Yes
OUTPUT "0"
S26
OUTPUT "1"
S27
LOGICAL ADDRESS = [40 0000]~[7F FFFF] ?
S28
No
Yes
PHYSICAL ADDRESS= LOGICAL ADDRESS- [40 0000]
S29
THRESHOLD VOLTAGE<3.5V ?
S30
No
Yes
THRESHOLD VOLTAGE<1.5 V ?
S31
No
Yes
OUTPUT "0"
S32
OUTPUT "1"
S33
THRESHOLD VOLTAGE<1.5 V ?
S34
No
Yes
OUTPUT "0"
S39
OUTPUT "1"
S40
PHYSICAL ADDRESS= LOGICAL ADDRESS- [80 0000]
S35
THRESHOLD VOLTAGE<3.5V ?
S36
No
Yes
THRESHOLD VOLTAGE<1.5V ?
S37
No
Yes
THRESHOLD VOLTAGE<0.5V ?
S38
Yes
THRESHOLD VOLTAGE<2.5V ?
S41
No
Yes
THRESHOLD VOLTAGE<5.5V ?
S42
No
Yes
THRESHOLD VOLTAGE<4.5V ?
S43
No
Yes
THRESHOLD VOLTAGE<6.5V ?
S44
No
Yes

FIG10

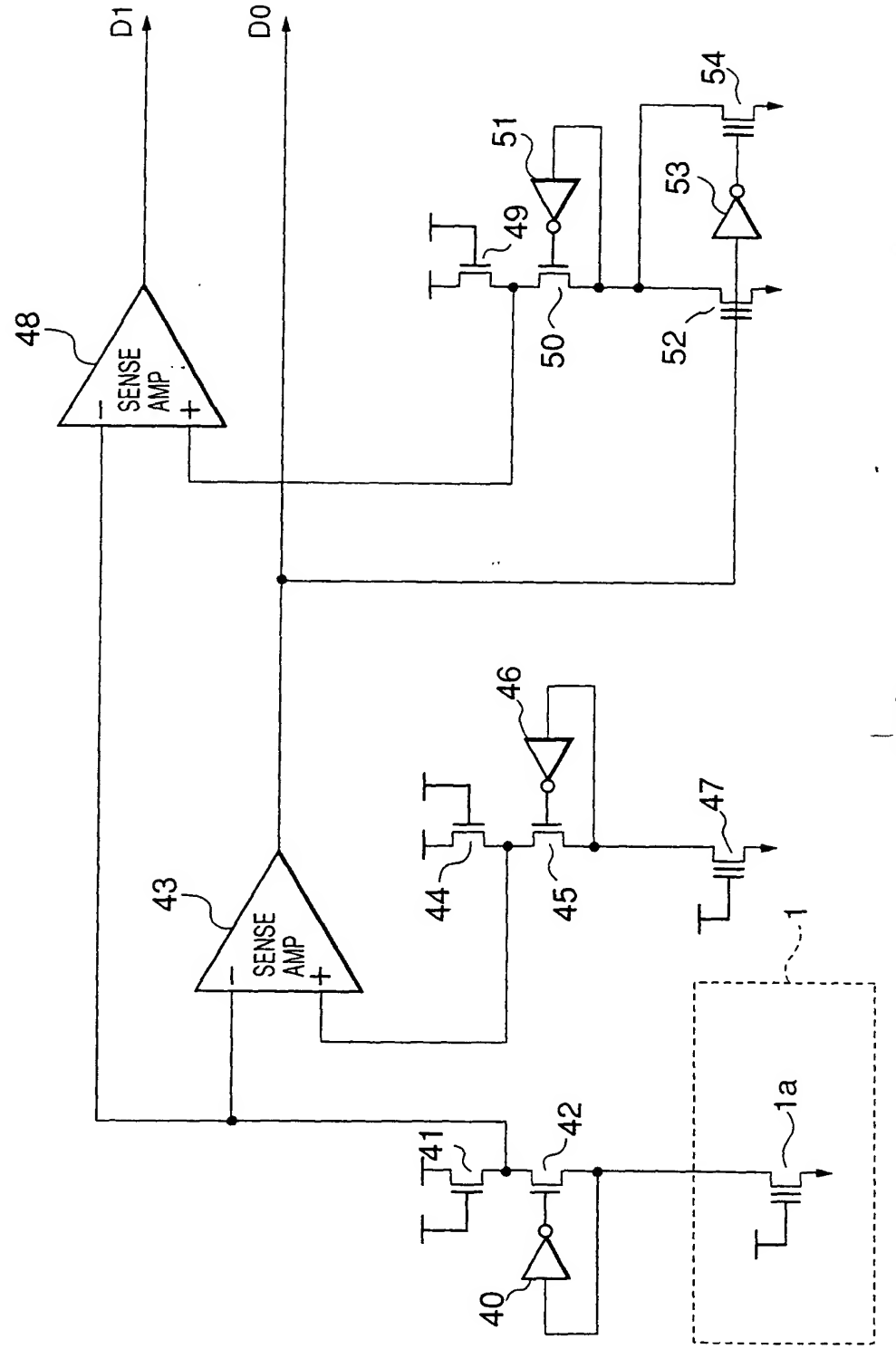
D1
D0
48
SENSE AMP
43
SENSE AMP
40
41
42
44
45
46
47
49
50
51
52
53
54
1
1a

FIG.11